R&E International

RE46C143

CMOS Photoelectric Smoke Detector ASIC with Interconnect

Product Specification

General Description

The RE46C143 is low power CMOS photoelectric type smoke detector IC. With minimal external components this circuit will provide all the required features for a photoelectric type smoke detector.

The design incorporates a gain selectable photo amplifier for use with an infrared emitter/detector pair. An internal oscillator strobes power to the smoke detection circuitry for 100us every 8.1 seconds to keep standby current to a minimum. If smoke is sensed the detection rate is increased to verify an alarm condition. A high gain mode is available for push button chamber testing.

A check for a low battery condition and chamber integrity is performed every 40 seconds when in standby. The alarm horn pattern utilizes a 75% duty cycle.

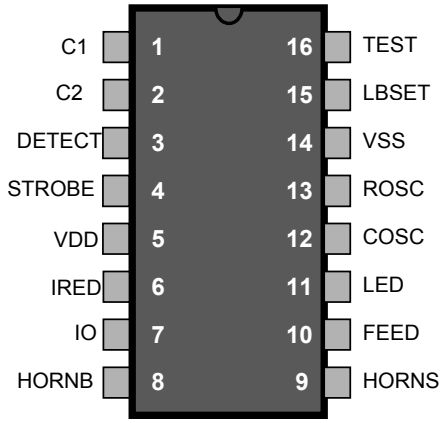
An interconnect pin allows multiple detectors to be connected such that when one units alarms, all units will sound.

Utilizing low power CMOS technology the RE46C143 was designed for use in smoke detectors that comply with Underwriters Laboratory Specification UL217 and UL268.

Features

- Internal Power On Reset
- Low Quiescent Current Consumption
- Available in 16L PDIP or 16L N SOIC
- ESD Protection on all Pins
- Interconnect up to 40 Detectors
- 75% Duty Cycle Horn Pattern
- Low Battery and Chamber Test
- Compatible with Motorola MC145010
- Available in Standard Packaging or RoHS Compliant Pb Free Packaging.

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{DD}	12.5	V
Input Voltage Range Except FEED, IO	V_{in}	-.3 to V_{dd} +.3	V
FEED Input Voltage Range	V_{infd}	-10 to +22	V
IO Input Voltage Range	V_{io1}	-.3 to +17	V
Input Current except FEED	I_{in}	10	mA
Operating Temperature	T_A	-25 to 75	°C
Storage Temperature	T_{STG}	-55 to 125	°C
Maximum Junction Temperature	T_J	150	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation at these conditions for extended periods may affect device reliability.

This product utilizes CMOS technology with static protection; however proper ESD prevention procedures should be used when handling this product. Damage can occur when exposed to extremely high static electrical charge.

DC Electrical Characteristics at TA = -25° to 75°C, VDD=9V, Typical Application (unless otherwise noted)

Parameter	Symbol	Test Pin	Test Conditions	Limits			
				Min	Typ	Max	Units
Supply Voltage	V_{DD}	5	Operating	6		12	V
Supply Current	I_{DD1}	5	Configured as in Figure 2, COSC=VSS		4	6	uA
	I_{DD2}	5	Configured as in Figure 2, VDD=12V, COSC=VSS		5.5	8	uA
	I_{DD3}	5	Configured as in Figure 2, STROBE on, IRED off, VDD=12V			2	mA
	I_{DD4}	5	Configured as in Figure 2, STROBE on, IRED on, VDD=12V, Note 1			3	mA
Input Voltage High	V_{IH1}	10	FEED	6.2	4.5		V
	V_{IH2}	7	No Local Alarm, IO as an Input	3.2			V
	V_{IH4}	16	TEST	8.5			V
Input Voltage Low	V_{IL1}	10	FEED		4.5	2.7	V
	V_{IL2}	7	No Local Alarm, IO as an Input			1.5	V
	V_{IL4}	16	TEST			7	V
Input Leakage Low	I_{IL1}	1,2,3	VDD=12V, COSC=12V, STROBE active			-100	nA
	I_{IL2}	12,15	VDD=12V, Vin=VSS			-100	nA
	I_{IL3}	16	VDD=12V, Vin=VSS			-1	uA
	I_{LFD}	10	FEED=-10V			-50	uA
Input Leakage High	I_{IH1}	1,2	VDD=12V, Vin=VDD, STROBE active			100	nA
	I_{IH2}	3,12,15	VDD=12V, Vin=VDD			100	nA
	I_{HFD}	10	FEED=22V			50	uA
Input Pull Down Current	I_{PD1}	16	Vin=VDD	.25		10	uA
	I_{PDIO1}	7	Vin=VDD	20		80	uA
	I_{PDIO2}	7	Vin=17V, VDD=12			140	uA
Output Leakage Current Low	I_{OZL1}	11,13	Output Off, Output=VSS			-1	uA
Output Leakage Current High	I_{OZH1}	11,13	Output Off, Output=VDD			1	uA

Note 1: Does not include Q3 emitter current.

DC Electrical Characteristics (continued) at TA= -25° to 75°, VDD=9V, Typical Application (unless otherwise noted)

Parameter	Symbol	Test Pin	Test Conditions	Limits			
				Min	Typ	Max	Units
Output Voltage Low	V_{OL1}	8,9	Iol=16mA, VDD=6.5V			1	V
	V_{OL2}	13	Iol=5mA, VDD=6.5V		.5		V
	V_{OL3}	11	Iol=10mA, VDD=6.5V			.6	V
Output Voltage High	V_{Oh1}	8,9	Ioh=-16mA, VDD=6.5V	5.5			V
Output Current	I_{IOH1}	7	Alarm, Vio=Vdd-2V or Vio=0V	-4		-16	mA
	I_{IODMP}	7	At Conclusion of Local Alarm or Test, Vio=1V	5			mA
Low Battery Alarm Voltage	V_{LB}	5	R14=100K, R15=47K, ILed=10mA	6.9	7.2	7.5	V
Output Voltage	V_{STOF}	4	STROBE off, VDD=12V, Iout=-1uA	V_{DD} - .1			V
	V_{STON}	4	STROBE on, VDD=9V Iout= 100uA to 500uA	V_{DD} - 5.3	V_{DD} - 5	V_{DD} - 4.7	V
	V_{IREDOF}	6	IRED off, VDD=12V, Iout=1uA			.1	V
	V_{IREDON}	6	IRED on, VDD=9V Iout=0 to -6mA, Ta=25C	2.25	3.1	3.75	V
Common Mode Voltage	V_{CM1}	1,2,3	Local smoke, Push to Test or Chamber Test, Note 1	.5		V_{DD}-2	V
Smoke Compare Reference	V_{ref}	-	Internal Reference	V_{DD}- 3.85		V_{DD}- 3.15	V
Temperature Coefficient	TC_{ST}	4	VDD=6V to 12V, STROBE Output Voltage		.01		%/ºC
	TC_{IRED}	6	VDD=6V to 12V, IRED Output Voltage		.3		%/ºC
Line Regulation	ΔV_{STON}	4,5	Active, VDD=6V to 12V		-50		dB
	ΔV_{IREDON}	6,5	Active, VDD=6V to 12V		-30		dB

Note 1: Not production tested
Typical values are for design information and are not guaranteed.
Limits over the specified temperature range are not production tested and are based on characterization data.

AC Electrical Characteristics at TA =-25° to 75°, VDD=9V, VSS=0V, Component Values from Figure 2 ; R9=100KΩ, R12=10MΩ, C5= 1.5nF(unless otherwise noted)

Parameter	Symbol	Test Pin	Test Conditions	Limits			
				Min	Typ	Max	Units
Oscillator Period	T_{POSC}	12	No Alarm Condition, Note 2	9.4	10.5	11.5	mS
LED and STROBE On Time	T_{ON1}	11,4	Operating	9.4	10.5	11.5	mS
LED Period	T_{PLED1}	11	Standby, No Alarm	38	43	47	S
	T_{PLED2}	11	Local Alarm Condition	.6	.67	.74	S
	T_{PLED4}	11	Remote Alarm Only	LED IS NOT ON			S
STROBE and IRED Pulse Period	T_{PER1}	4,6	Standby, No Alarm	9.7	10.5	11.8	S
	T_{PER1A}	4,6	Standby, After 1 Valid Smoke Sample	2.42	2.7	2.96	S
	T_{PER1B}	4,6	Standby, After 2 Consecutive Valid Smoke Samples	1.21	1.33	1.47	S
	T_{PER2}	4,6	In Local Alarm – (3 Consecutive Valid Smoke Samples)	1.21	1.33	1.47	S
	T_{PER3}	4,6	In Remote Alarm	9.7	10.5	11.8	S
	T_{PER4}	4,6	Pushbutton Test		336		mS
	T_{PER5}	4,6	Chamber Test or Low Battery Test, no Alarms	39		47	S
IRED On Time	T_{ON2}	6	Operating, Note 2	94	104	115	uS
Horn On Time	T_{HON1}	8,9	Operating, Alarm Condition, Note 1	227	252	277	mS
	T_{HON2}	8,9	Low Battery or Failed Chamber Test , No Alarm	9.5	10.5	11.5	mS
Horn Off Time	T_{HOF1}	8,9	Operating, Alarm Condition, Note 1	76	84	92	mS
	T_{HOF3}	8,9	Low Battery or Failed Chamber Test, No Alarm	39	43	47	S
IO Charge Dump Duration	T_{IODMP}	7	At Conclusion of Local Alarm or Test	.91		1.46	S
IO Delay	T_{IODLY1}	7	From Start of Local Alarm to IO Active		0		S
IO Filter	T_{IOFILT}	7	IO pulse width guaranteed to be filtered. IO as Input, No Local Alarm			600	mS
Remote Alarm Delay	T_{IODLY2}	7	No Local Alarm, From IO Active Horn Active	.75		1.65	S

Note 1 – See timing diagram for Horn Temporal Pattern
Note 2 - T_{POSC} and T_{ON2} are 100% production tested. All other timing is guaranteed by functional testing.

Typical values are for design information and are not guaranteed.
Limits over the specified temperature range are not production tested and are based on characterization data.

Functional Block Diagram

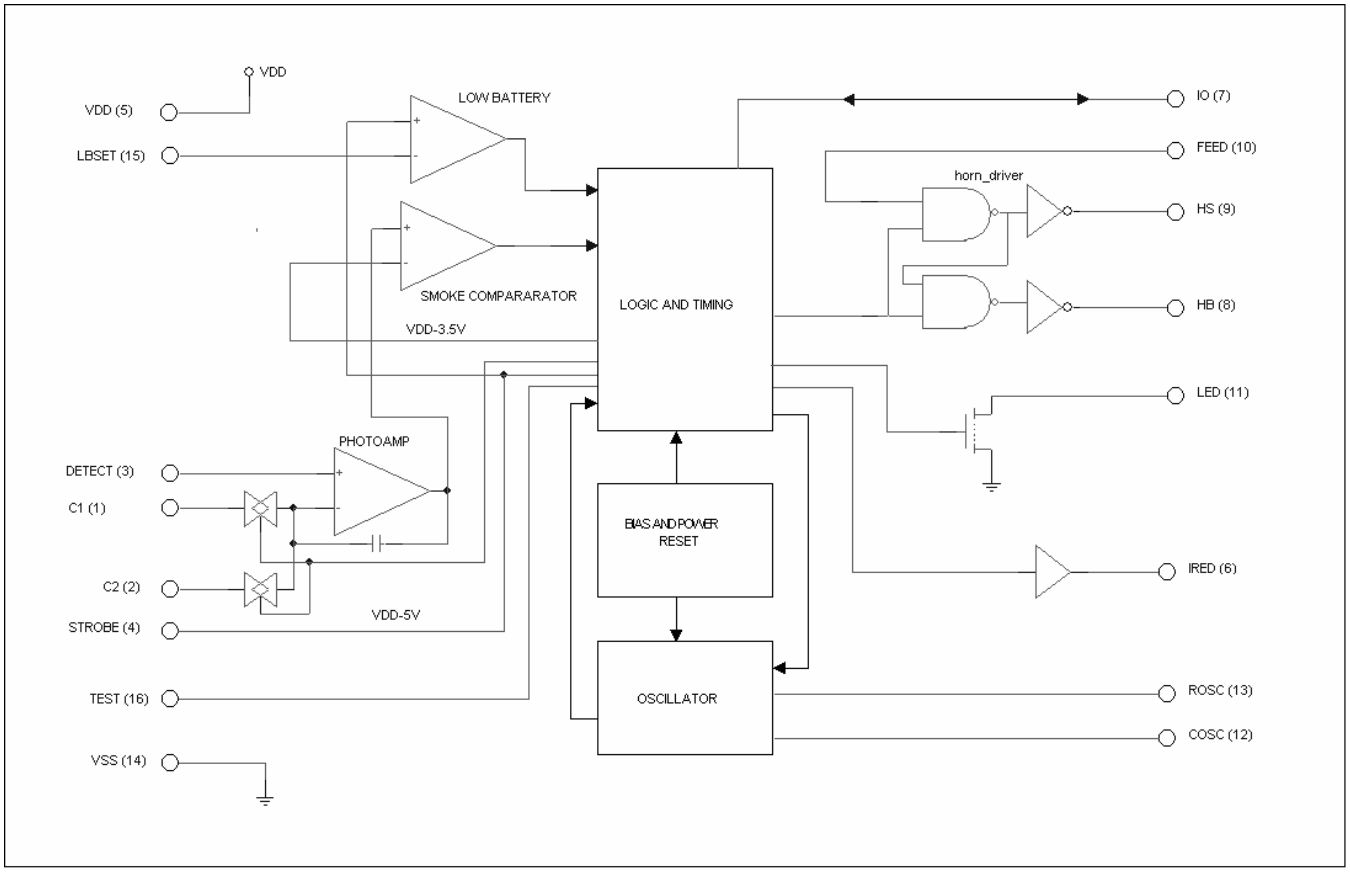


Figure 1

PIN DESCRIPTIONS

PIN#	PIN NAME	DESCRIPTION
1	C1	The capacitor connected to this pin sets the photo amplifier gain (high) for the push-to-test and chamber sensitivity test. The size of this capacitor will depend on the chamber background reflections. A=1+(C1/10) where C1 is in pF. The gain should be <10000.
2	C2	The capacitor connected to this pin sets the photo amplifier gain (normal) during standby. The value of this capacitor will depend on the smoke sensitivity required. A=1+(C2/10) where C2 is in pF.
3	DETECT	Positive input to the photo amplifier. This input is normally connected to the cathode of an external photo diode operated at zero bias.
4	STROBE	Regulated output voltage of VDD-5 which is active during a test for smoke. This output is the negative side of the photo amplifier circuitry.
5	VDD	Connect to the positive supply voltage
6	IRED	Provides a regulated pulsed output voltage pre-driver for the infrared emitter. This output usually drives the base of an NPN transistor.
7	IO	This bidirectional pin provides the capability to interconnect many detectors in a single system. This pin has an internal pull-down device.
8	HB	This pin is connected to the metal electrode of a piezoelectric transducer.
9	HS	HS is a complementary output to HB and connects to the ceramic electrode of the piezoelectric transducer.
10	FEED	Usually connected to the feedback electrode through a current limiting resistor. If not used this pin must be connected to VDD or VSS.
11	LED	Open drain NMOS output used to drive a visible LED.
12	COSC	A capacitor connected to this pin with a parallel resistor sets the internal clock low time which is approximately the clock period.
13	ROSC	A resistor between this pin and pin 12 (COSC) sets the internal clock high time. This also sets the IRED pulse width (100-200uS).
14	VSS	Connect to the negative supply voltage.
15	LBSET	This input is connected to a VDD reference voltage to set the low battery warning voltage.
16	TEST	This input is used to invoke two test modes. This input has an internal pull-down.

Typical Application

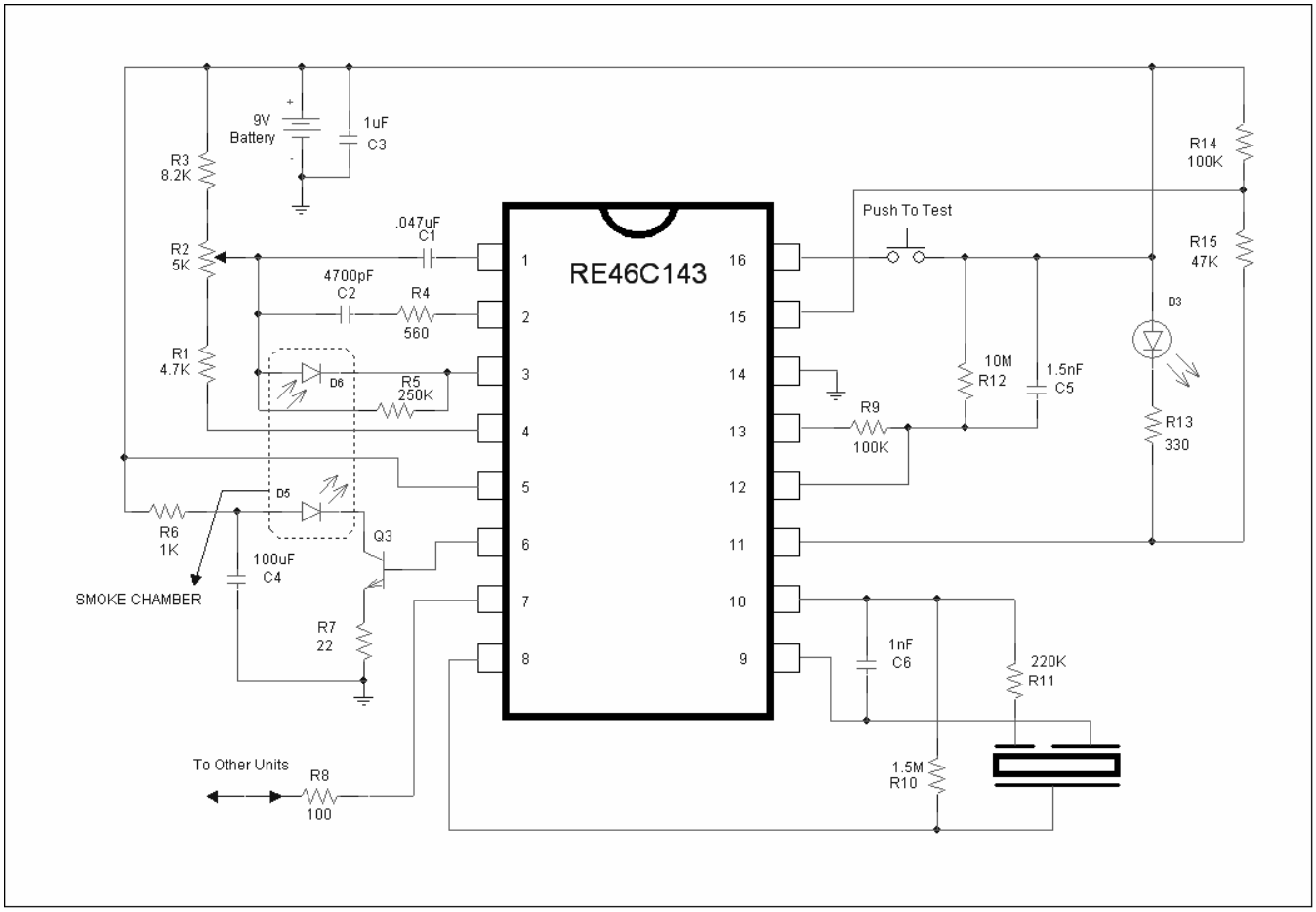


Figure 2

Notes:

1. C3 should be located as close as possible to the device power pins.
2. C3 is typical for an alkaline battery. This capacitance should be increased to 4.7uF or greater for a carbon battery.
3. R10, R11 and C6 are typical values and may be adjusted to maximize sound pressure.

CIRCUIT DESCRIPTION AND APPLICATION NOTES

Note: All timing references are nominal. See electrical characteristics for limits.

Standby Internal Timing – With the external components specified in the typical application figure for ROSC and COSC the internal oscillator has a nominal period of 10mS. Normally the analog circuitry is powered down to minimize standby current (typically 4uA at 9V). Once every 10 seconds the detection circuitry (normal gain) is powered up for 10mS. Prior to completion of the 10mS period the IRED pulse is active for 100uS. At the conclusion of this 10mS period the photo amplifier is compared to an internal reference to determine the chamber status and latched. If a smoke condition is present the period to the next detection decreases and additional checks are made. Three consecutive smoke detections will cause the device to go into alarm and the horn circuit and interconnect will be active.

Once every 40 seconds the status of the battery voltage is checked. This status is checked and latched at the conclusion of the LED pulse. In addition, once every 40 seconds the chamber is activated and using the high gain mode (capacitor C1) a check of the chamber is made by amplifying background reflections. If either the low battery or the photo chamber test fails the horn will chirp for 10mS every 40 seconds.

The oscillator period is determined by the values of R9, R12 and C5 (see typical application FIG 2). The oscillator period $T=T_R+ T_F$ where T_R =.6931 * R12 * C5 and T_F =.6931 * R9 * C5

Smoke Detection Circuitry – A comparator compares the photo amp output to an internal reference voltage. If the required number of consecutive smoke conditions is met the device will go into local alarm and the horn will be active. In local alarm the C2 gain is internally increased by ~10% to provide alarm hysteresis.

Push to Test Operation – If the TEST input pin is activated (Vih) then, after one internal clock cycle, the smoke detection rate increases to once every 330mS. In this mode the high gain capacitor C1 is selected and background reflections are used to simulate a smoke condition. After the required consecutive detections the device will go into a local alarm condition. When the TEST input is deactivated (Vil) and after one clock cycle the normal gain capacitor C1 is selected. The detection rate continues at once every 330mS until 3 consecutive no smoke conditions are detected. At this point the device returns to standby timing.

LED Operation – In standby the LED is pulsed on for 10mS every 40 seconds. In a local alarm condition or the push to test alarm the LED pulse frequency is increased to once every 0.5 seconds. In the case of a remote alarm the LED not active.

Interconnect Operation – The bidirectional IO pin allows for interconnection of multiple detectors. In a local alarm condition this pin is driven high immediately through a constant current source. Shorting this output to ground will not cause excessive current. The IO is ignored as an input during a local alarm.

The IO pin also has an NMOS discharge device that is active for ~1 second after the conclusion of any type of local alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote active high signal is detected the device goes into remote alarm and the horn will be active. Internal protection circuitry allows for the signaling unit to have a higher supply voltage than the signaled unit without excessive current draw.

The interconnect input has a 500mS nominal digital filter. This allows for interconnection to other types of alarms (carbon monoxide for example) that may have a pulsed interconnect signal.

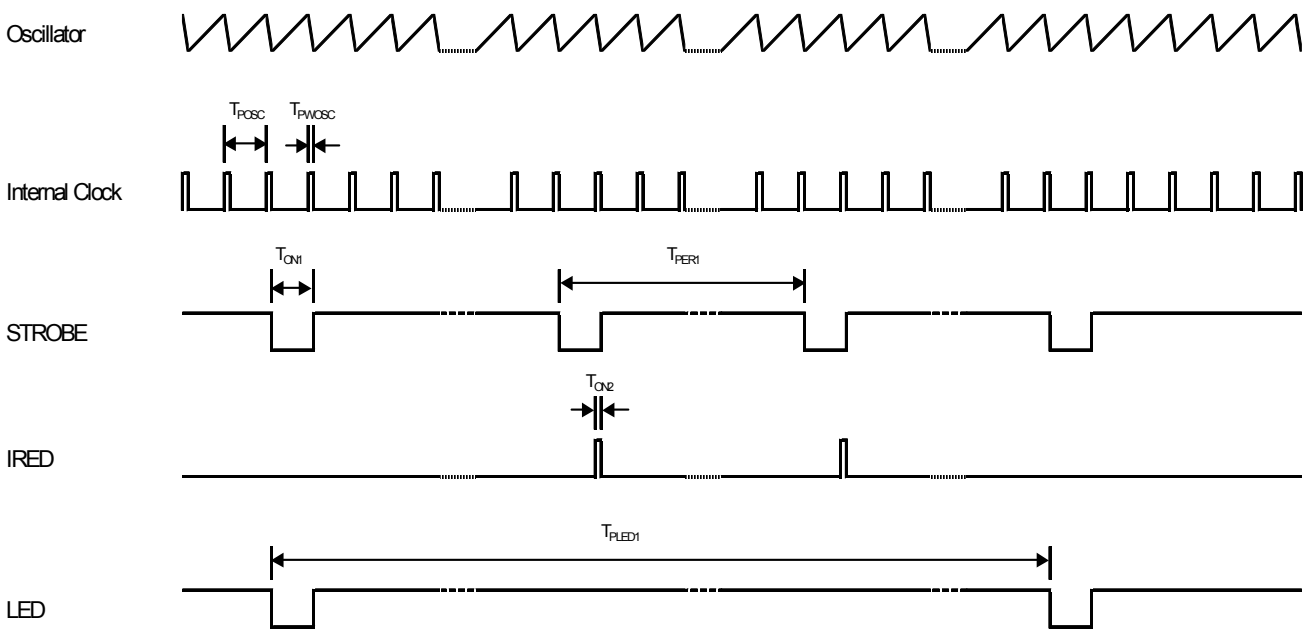
Low Battery and Chamber Test – In standby an internal reference is compared to the voltage divided VDD supply. Low battery status is latched at the conclusion of the LED pulse. The horn will chirp for 10ms every 40 seconds until the low battery condition no longer exists. In standby a chamber test is also performed every 40 seconds by switching to the high gain capacitor C1 and sensing the photo chamber background reflections. Two consecutive chamber tests failures will also cause the horn to chirp for 10mS every 40 seconds. The low battery chirp occurs next to the LED pulse and the failed chamber test chirp 20 seconds later. The low battery and chamber tests are not performed in a local or remote alarm condition. The low battery alarm threshold is approximately equal to ((5*R15)/R14)+5 where R15 and R16 are in the same units.

Diagnostic Mode – In addition to the normal function of the TEST input a special diagnostic mode is available for calibration and test of the smoke detector. Taking the TEST pin below VSS and sourcing ~300uA out of the pin for 1 clock cycle will enable the diagnostic mode. In the diagnostic mode some of the pin functions are redefined. Refer to the table below for redefined pin functions in the diagnostic mode. In addition in this mode STROBE is always enabled and the IRED is pulsed at the clock rate of 10mS nominal.

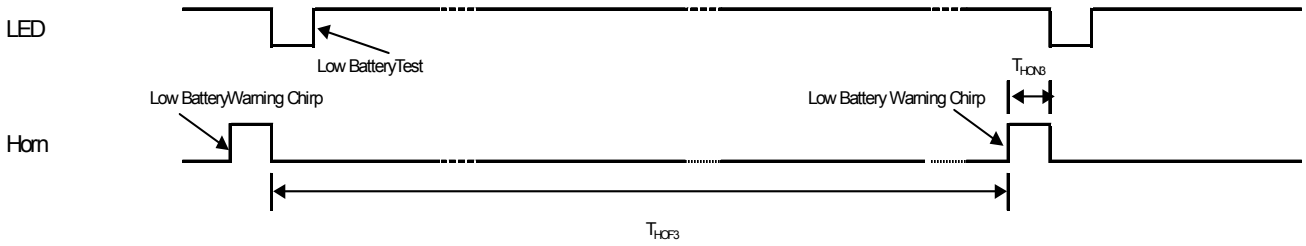
Pin Name	Pin Number	Description
IO	7	Disabled as an output. A high on this pin directs the photo amplifier output to pin C1 (1) or C2 (2), determined by the level on LBSET (15). Amplification occurs during the IRED active time.
LBSET	15	If IO is high then this pin controls the gain capacitor that is used. If LBSET is low then normal gain is selected and the photo amp output appears on C1 (1). If LBSET is high then high gain is selected and the photo amp output is on C2 (2).
FEED	10	If LBSET (15) is low then taking this input high will enable hysteresis, which is a nominal 10% gain increase in normal gain mode.
COSC	12	If desired this pin can be driven by an external clock.
HORNB	8	This pin becomes the smoke integrator output. A high level indicates that an alarm condition has been detected.
LED	11	The LED pin is used as a low battery indicator. For VDD above the low battery threshold the open drain NMOS is off. If VDD falls below the threshold the NMOS turns on.

Timing Diagrams

Standby, No Alarm (not to scale)



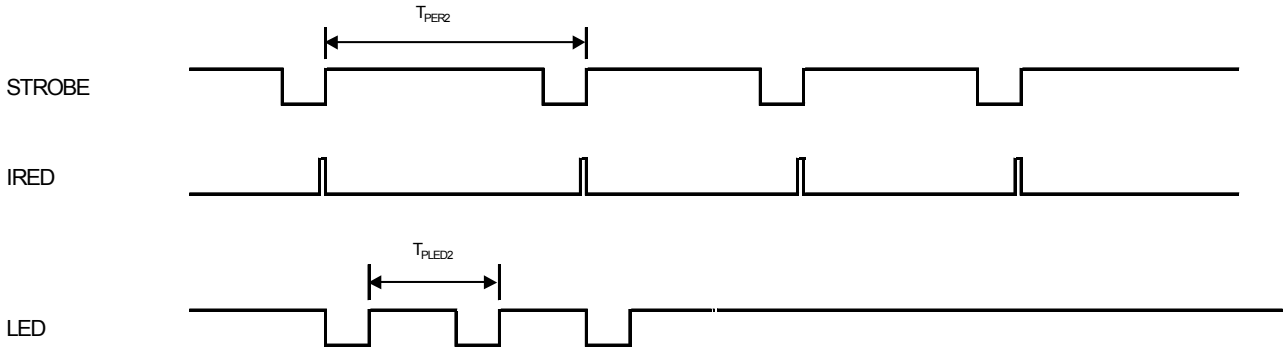
Low Supply or Chamber Test Failure



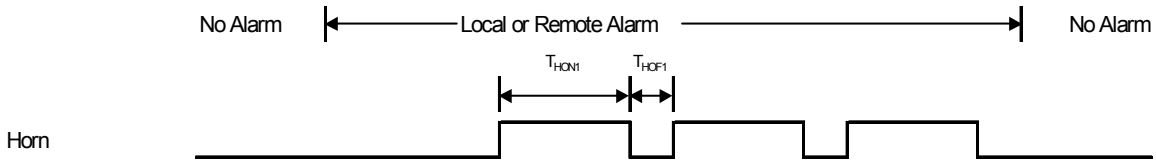
Chamber Test and Warning is Offset from Low Battery Test and Warning by 21.5 Seconds

Timing Diagrams (continued)

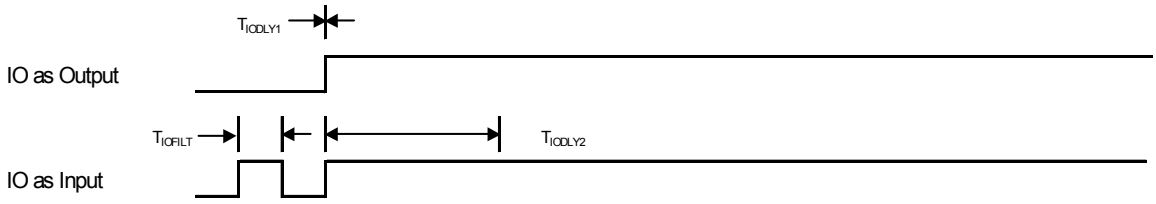
Local Alarm Timing (not to scale)



Horn Timing



Interconnect Timing



Notes:

1. Smoke is not sampled when the horn is active. Horn cycle is self completing in local alarm.
2. Low battery warning chirp is suppressed in local or remote alarm
3. IO Dump active only in local alarm, inactive if external alarm

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